Notice of References Cited	Application/Control No. 09/783,246	Applicant(s)/Patent Under Reexamination HUTTON, MICHAEL D.	
	Examiner Thomas H. Stevens	Art Unit 2123	Page 1 of 2

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Hutton et al., "Equivalence Classes of Clone Circuits for Physical-Design Benchmarking" 1999. pg.VI-428 to VI-431 IEEE.
	V	Hutton et al., "Characterization and Parameterized Random Generation of Digital Circuits" 1996 DAC. pg.94-99.
	W	Hutton et al., "Applications of Clone Circuits to Issue in Physical-Design" 1999. pg.VI-448 to VI-451 IEEE.
	X	Wilton.S.J.E., "Heterogeneous Technology Mapping for Area Reduction in FPGA's with Embedded Memory Arrays" 2000. IEEE pg. 56-68.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Notice of References Cited	Application/Control No. 09/783,246	Applicant(s)/Patent Under Reexamination HUTTON, MICHAEL D.	
	Examiner Thomas H. Stevens	Art Unit 2123	Page 2 of 2

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Hutton et al., "Timing-Drivent Placement for Hierarchical Programmable Logic Devices" 2001. pg.3-11 FPGA 2001.
	V	Hutton et al., "Characterization and Parameterized Generation of Synthetic Combination Benchmark Circuits" 1998. pg. 985-996 IEEE.
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.